IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: WANG, Sung-Fei	Confirmation No: 7610
Appl. No.	: 10/809,384	
Filed	: March 26, 2004	
Title	: BUMP STRUCTURE OF A SEMICONDUCTOR WAFER AND MANUFACTURING METHOD THEREOF	
TC/A.U.	: 2826	
Examiner	: SANDVIK, Benjamin P.	
Docket No.:	: WANG3232/REF	
Customer No:	: 23364	

3/6/06 BPS

DO NOT ENTER

REQUEST FOR RECONSIDERATION

Mail Stop A/F
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is in response to the Official Action of October 5, 2005, in connection with the above-identified application. The period for response to this Official Action has been extended to expire on February 5, 2006, by the filing herewith of a petition for a One Month Extension of Time and payment of the required fee.

The Official Action has rejected claims 1-4, 6-16 and 18 under 35 U.S.C. §103(a) as being obvious over, at least in part, the combination of Nakamura and Yano. The Official Action urges that all of the elements of claim 1 are disclosed in Nakamura with the exception of a plurality of reinforced bumps interposed between the chip and the substrate with no electrically conductive function, wherein the reinforced bumps connect the first central area and the second central area. However, the Official Action notes that Yano teaches a configuration of solder ball electrodes wherein solder balls in the central area have no electrically conductive function. The Official Action continues that it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the package of Nakamura with solder balls to connect the first and second central area, wherein the solder balls have no electrically conductive function as taught by Yano in order to improve the heat transfer characteristics of the package. Applicants